**USF- EEL3705L: Fund of Digital Circuits Lab**

**Name: UID:**

**Lab 6: Designing counters and porting Verilog function module in FPGA.**

1. Write a module to implement a 4-bit counter using J-K flipflops in Verilog.

Please show the following

* Code
* Schematic
* Timing Diagram

**Port the Verilog modules in FPGA.**

1. Implement an odd counter 1-9 using a 4-bit counter (you have to use stopping condition)

Please show the following

* Code
* Schematic
* Timing Diagram

**Port the Verilog modules in FPGA.**